

MIMAS

DVT BUILD

2010-11-17

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2008/10/01	2008-ECO-016553	B
DATE	CHANGE NO.	REV

	EE	DATE	POWER	DATE	INVENTEC		
DRAWER	Bai, Brain	2008-AGU-25			TITLE MIMAS		
DESIGN	Bai, Brain	2008-AGU-25					
CHECK	Bai, Brain	2008-AGU-25			SIZE = 3 FILE NAME : XXXX-XXXXXX-XX P/N 6050A2215101		
RESPONSIBLE							
					SIZE	CODE	DOC. NUMBER
					A3	CS	6050A2350601
					REV X02		
					SHEET 1 OF 34		

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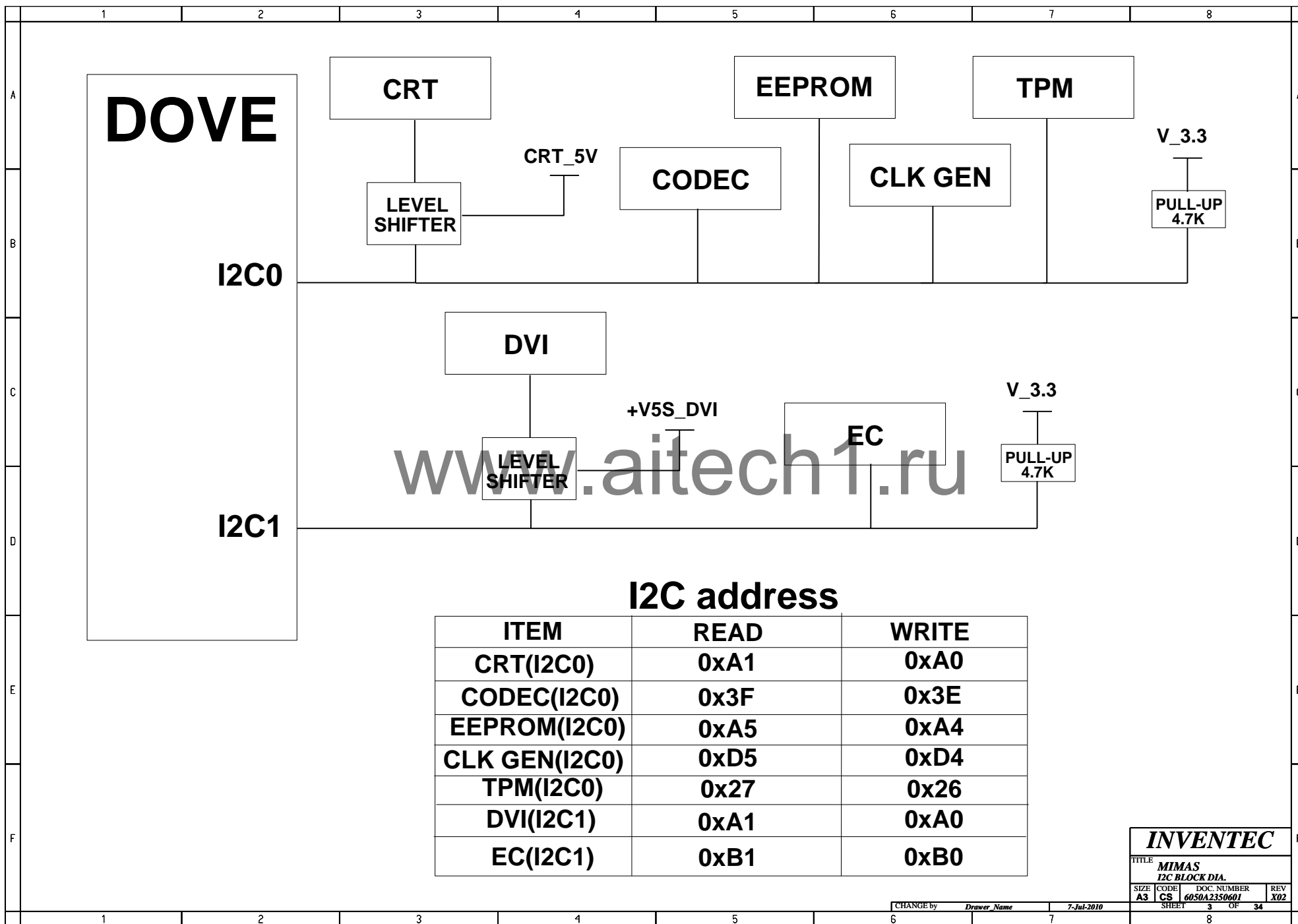
	PAGE
1. COVER PAGE	
2. INDEX	
3. I2C BLOCK DIAGRAM	
4. BLOCK DIAGRAM(DESKTOP)	
5. POWER SEQUENCE BLOCK	
6. DC JACK & VOLTAGE RESET	
7. 3.3V & 5.0V	
8. 1.8V & 2.5V	
9. 1.5V & VTT	
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15. DDR TERMINATOR	
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18. DVI TRANSMITTER	
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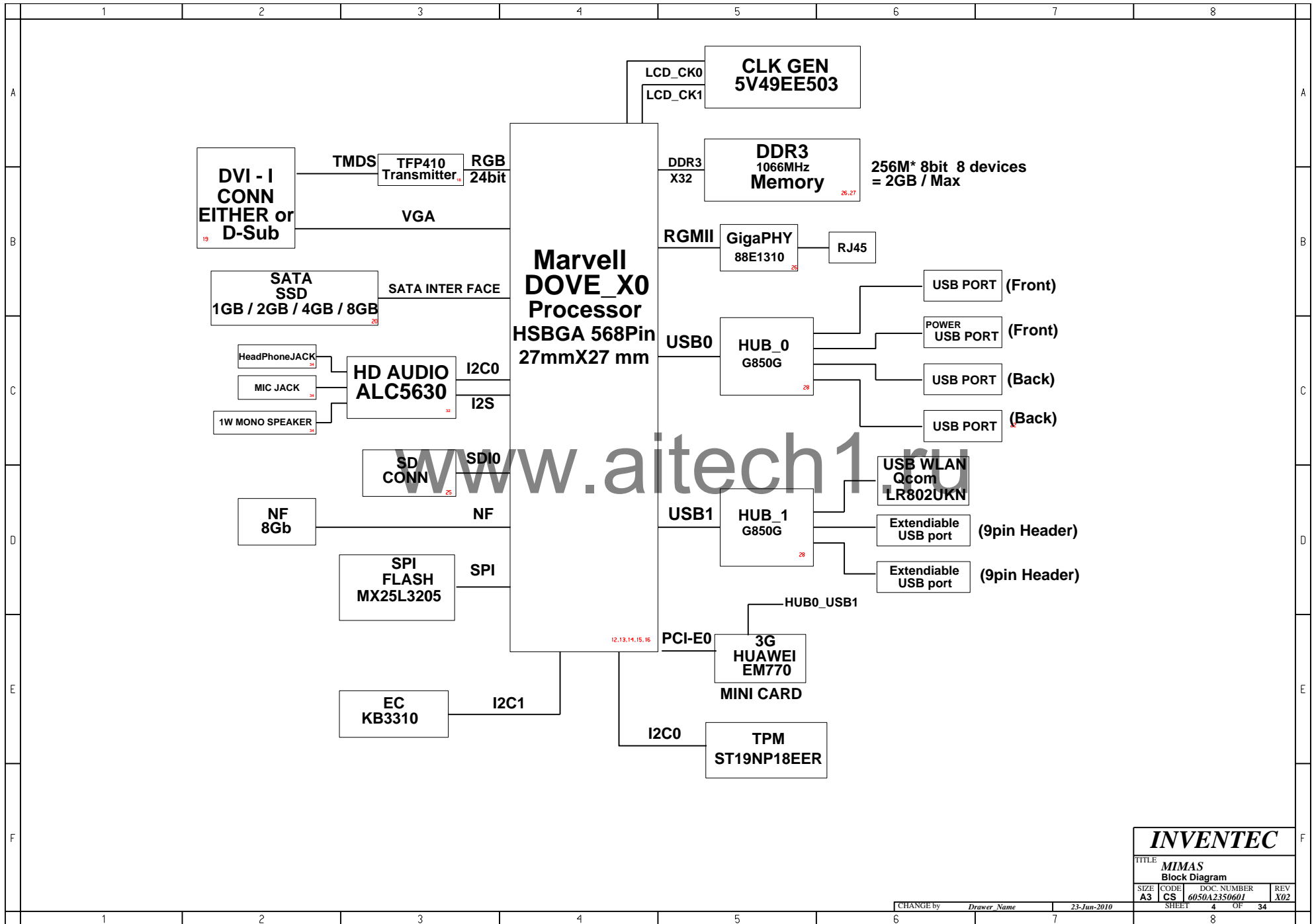
INVENTEC

TITLE
MIMAS

SIZE A3	CODE CS	DOC. NUMBER 6050A2350601	REV X02
SHEET 2		OF 34	

CHANGE by *Drawer Name* 7-Jun-2010

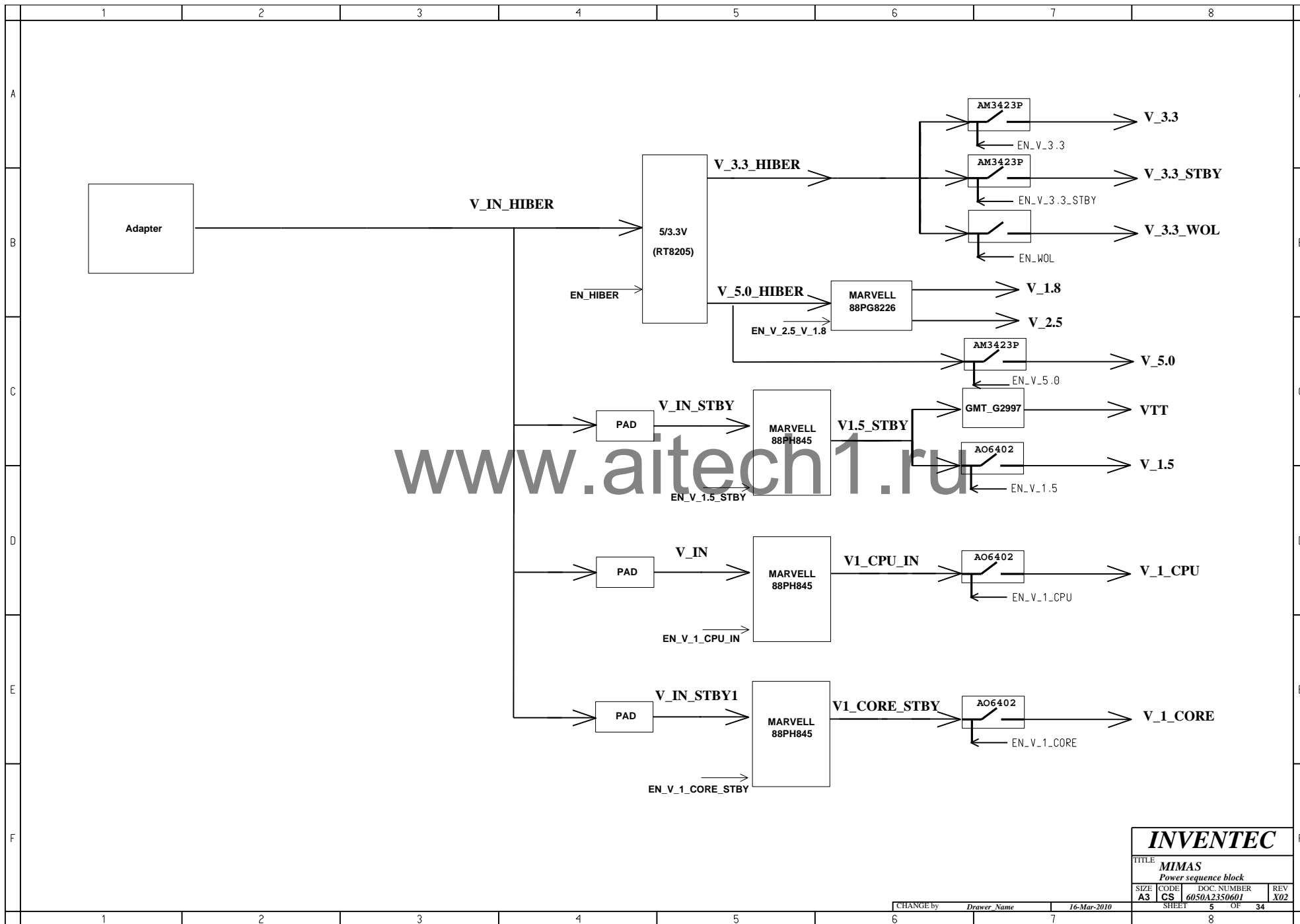




INVENTEC

TITLE			
MIMAS Block Diagram			
SIZE	CODE	DOC. NUMBER	REV
A3	CS	6050A2350601	X02
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CHANGE by *Drawer Name* 23-Jun-2010

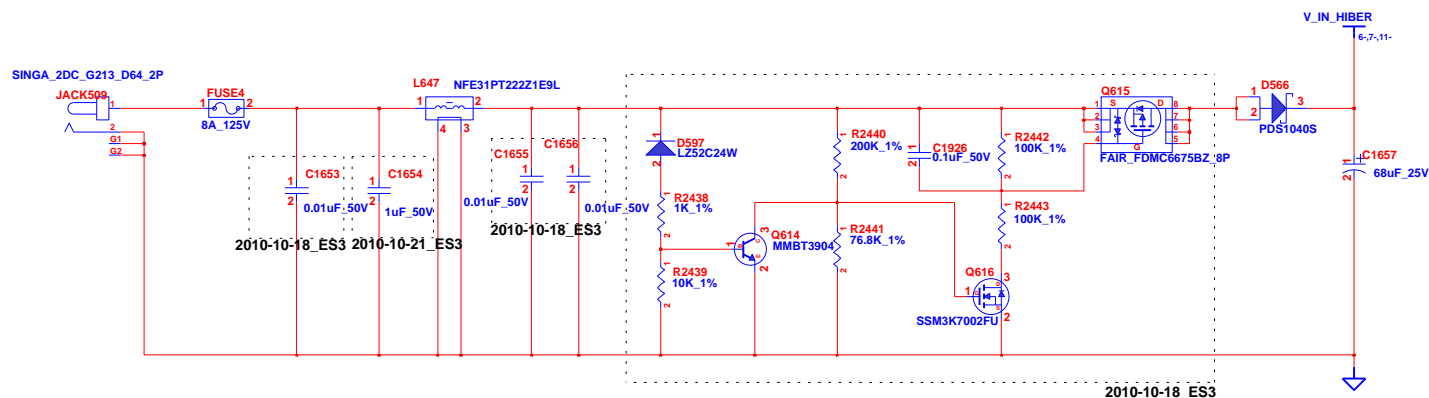


INVENTEC

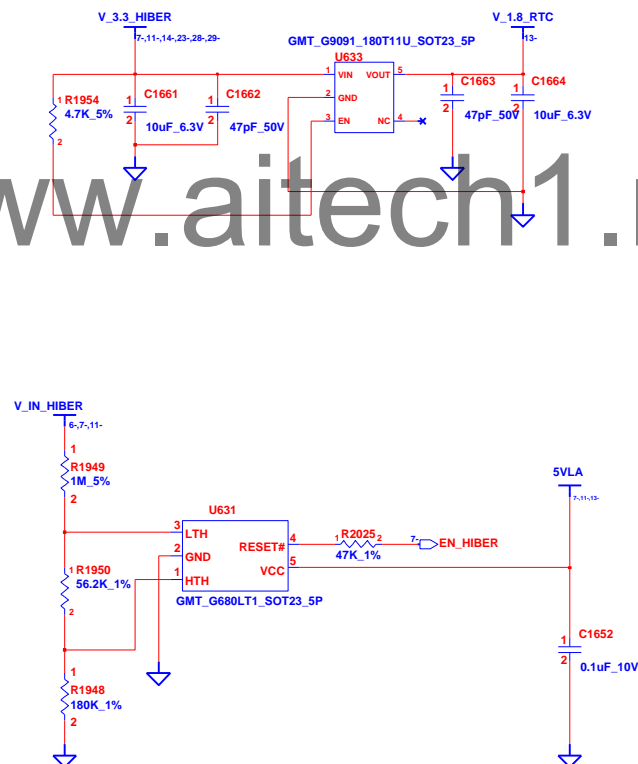
TITLE			
MIMAS			
Power sequence block			
SIZE	CODE	DOC. NUMBER	REV
A3	CS	6050A2350601	X02

CHANGE by *Drawer Name* 16-Mar-2010

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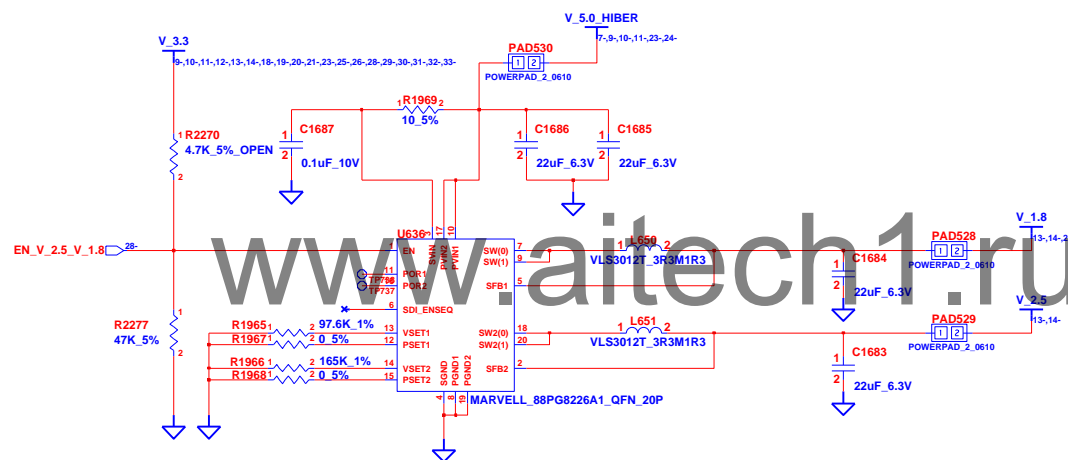


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INVENTEC			
TITLE			
MIMAS			
DC JACK & VOLTAGE RESET			
SIZE	CODE	DOC. NUMBER	REV
A3	CS	6050A2350601	X02
CHANGE by		Drawer Name	8-Sep-2010
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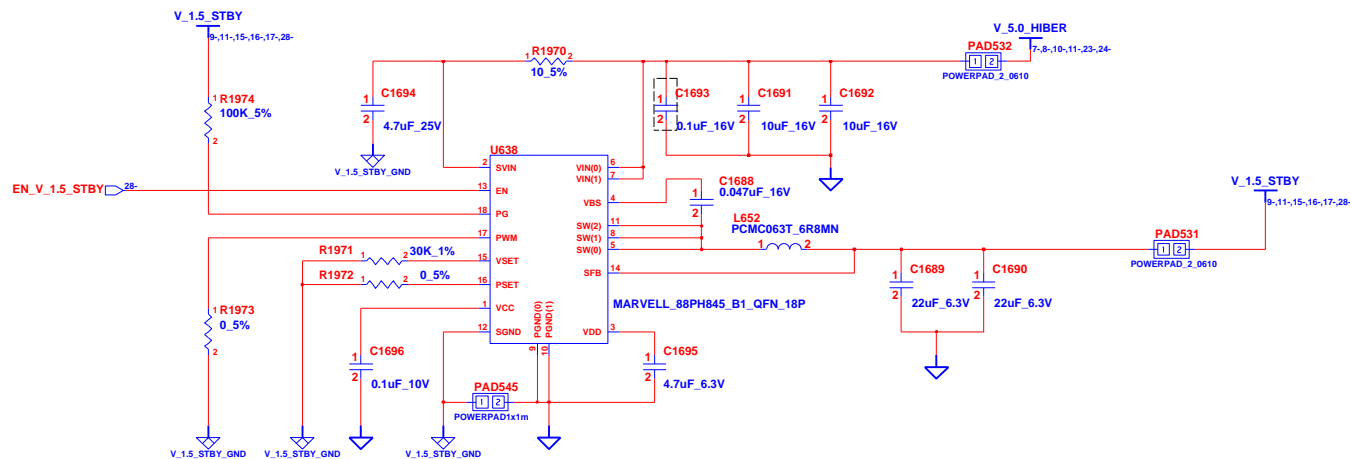
INVENTEC

TITLE
MIMAS
1.8V & 2.5V

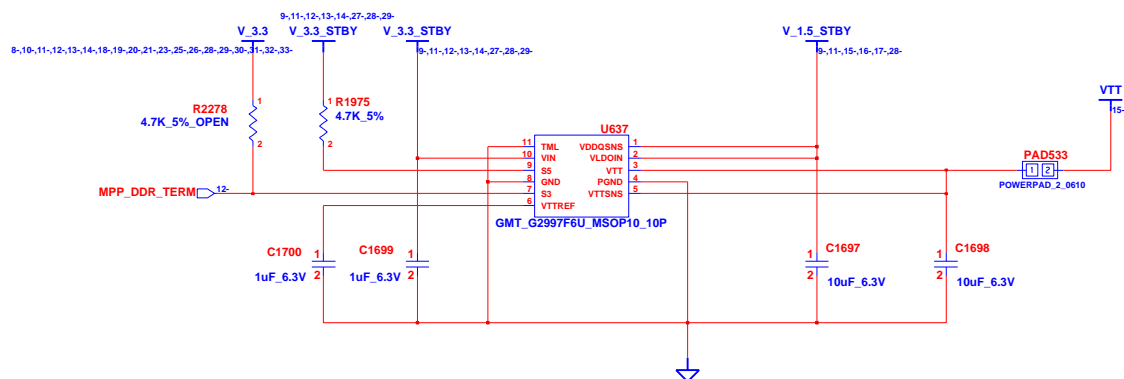
SIZE	CODE	DOC. NUMBER	REV
A3	CS	6050A2350601	X02

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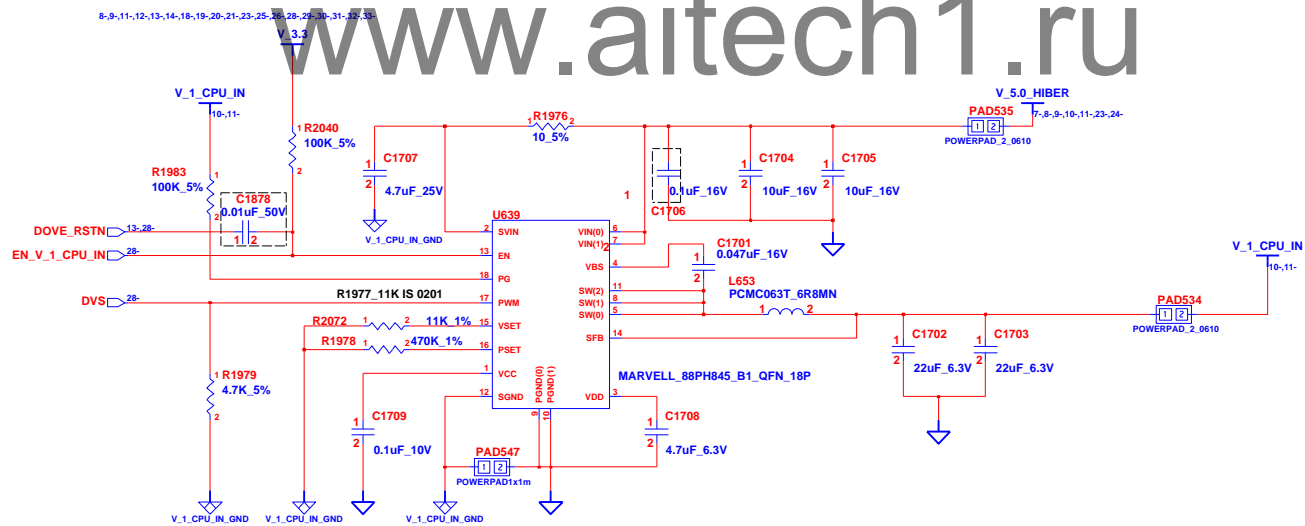
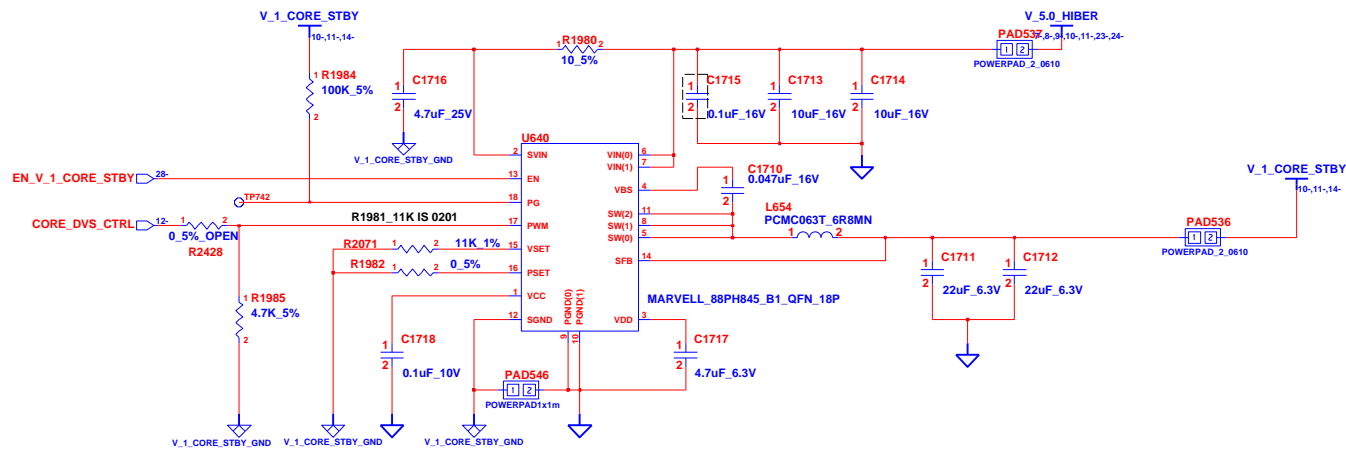
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INVENTEC			
TITLE			
MIMAS			
SYSTEM POWER (3V7 / 1V8 D161)			
SIZE	CODE	DOC. NUMBER	REV
A3	CS	6050A2350601	X02

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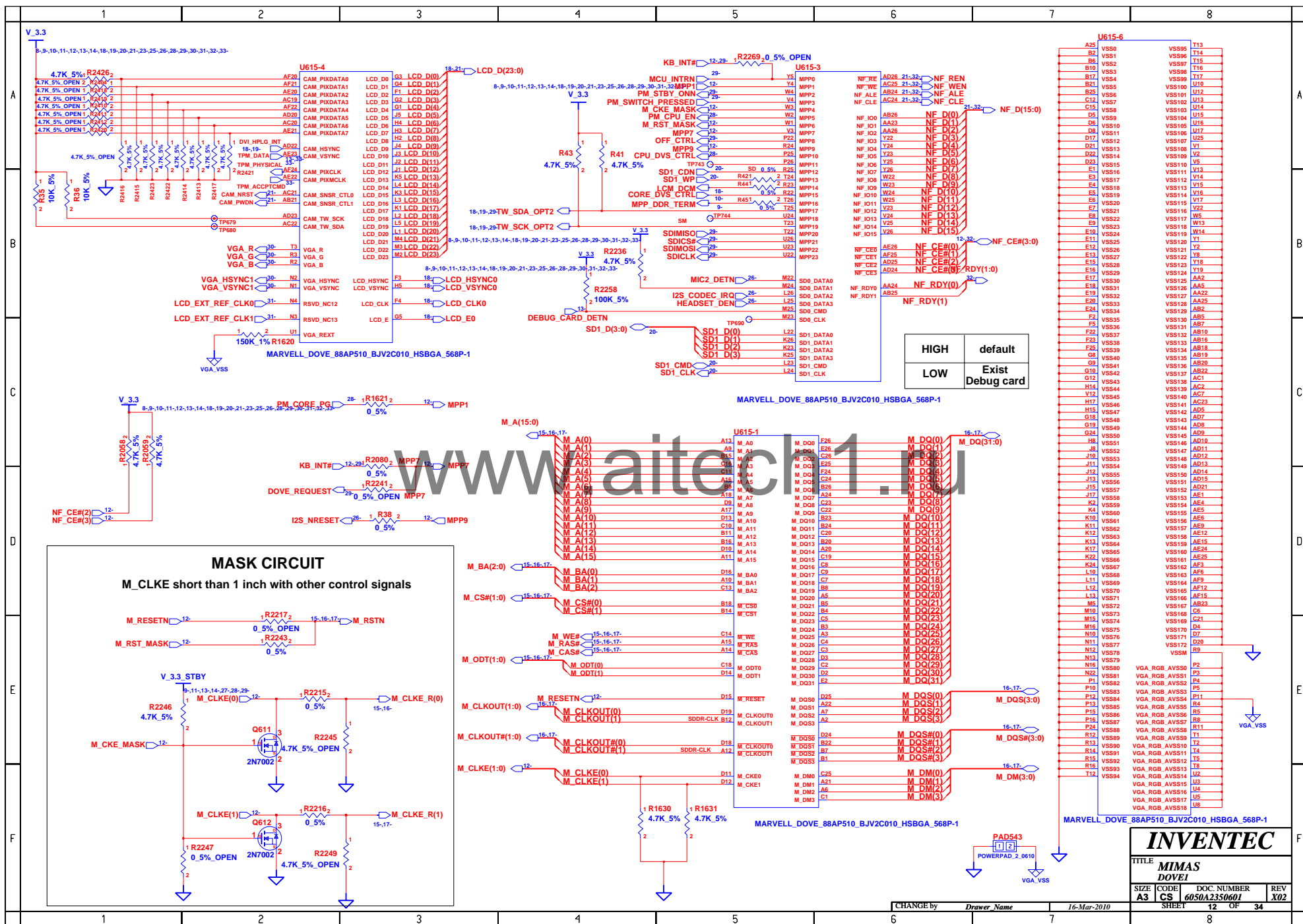
SHEET 9 OF 34

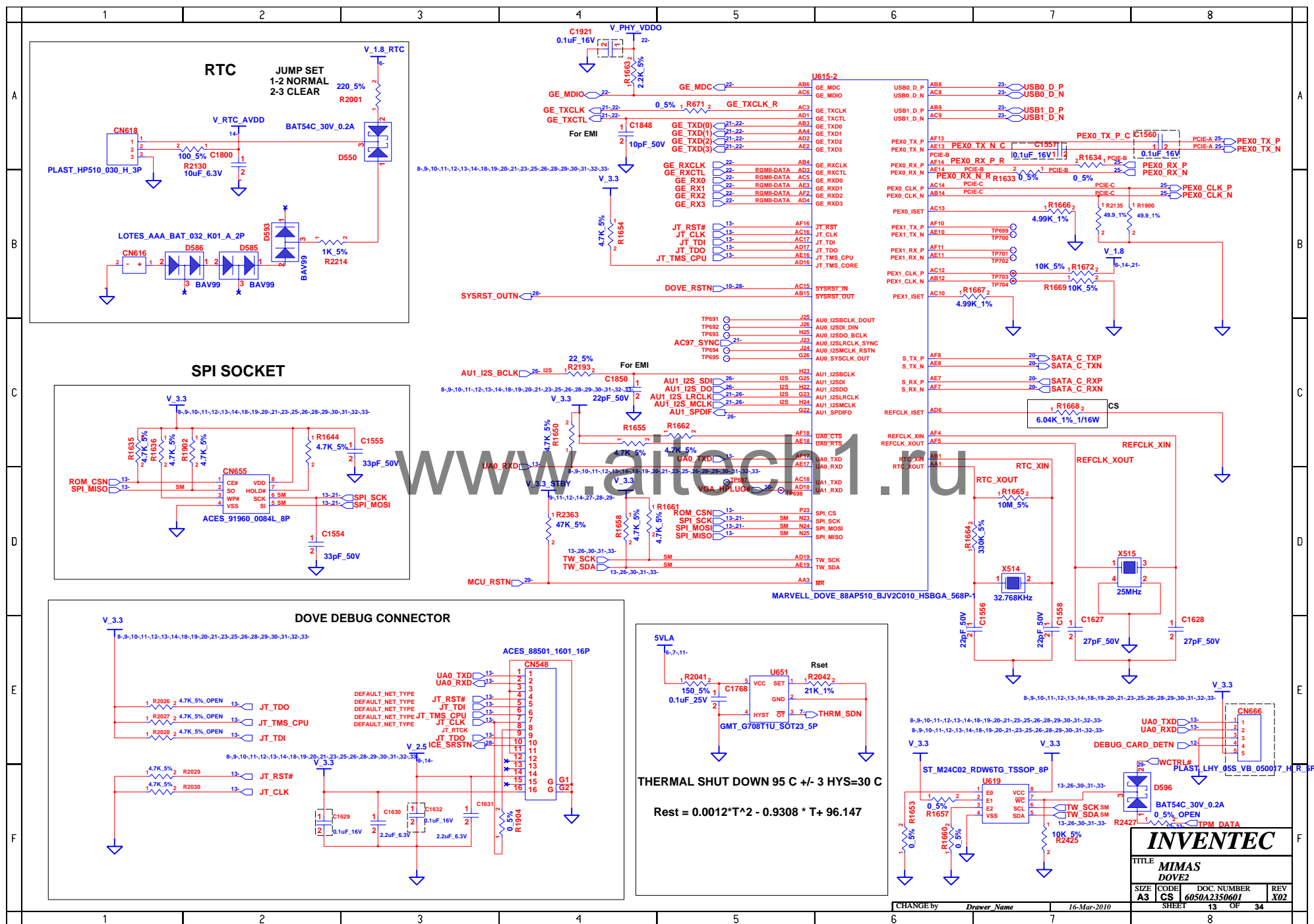


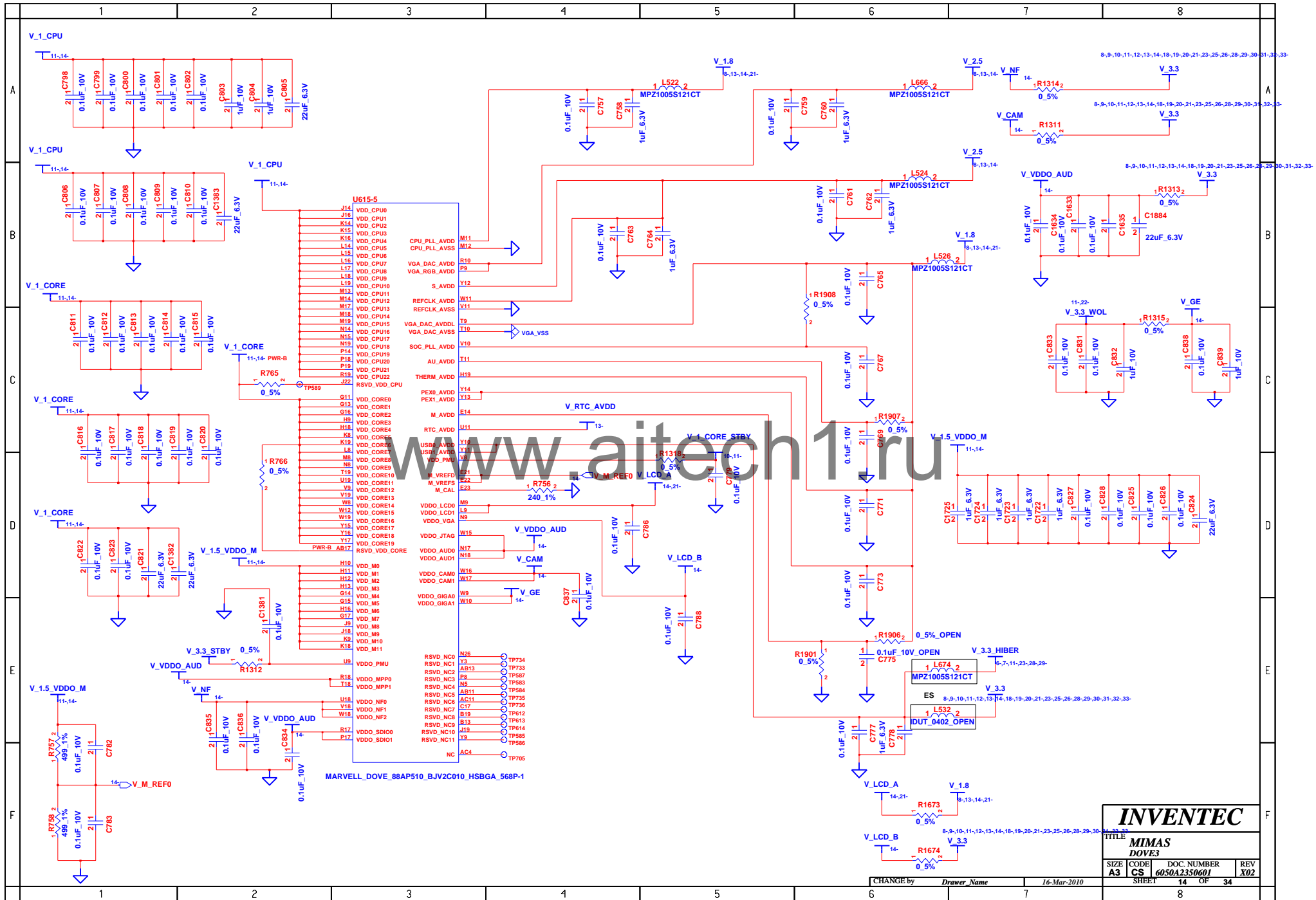
INVENTEC

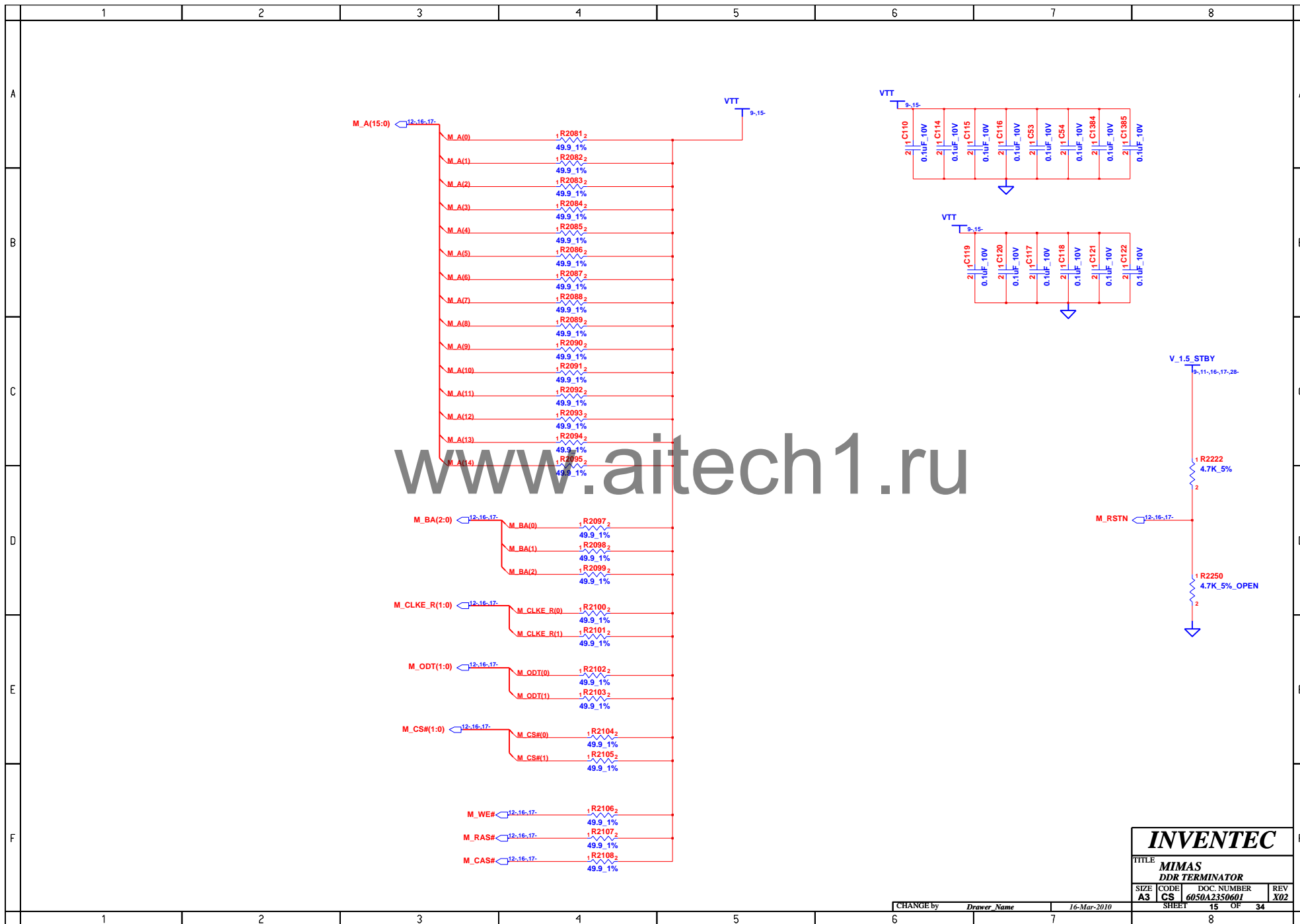
TITLE			
MIMAS			
VCORE & VCPU			
SIZE	CODE	DOC. NUMBER	REV
A3	CS	6050A2350601	X02
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INVENTEC

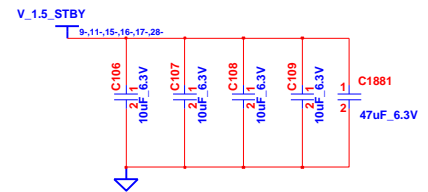
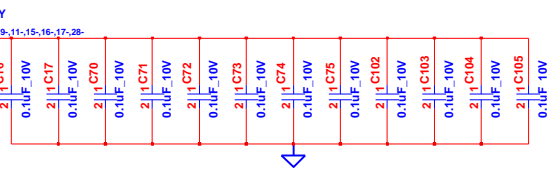
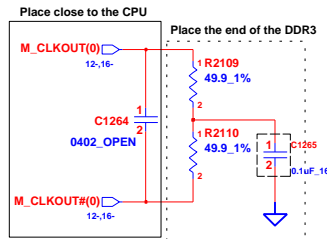
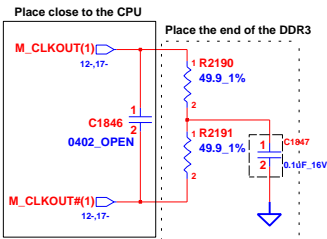
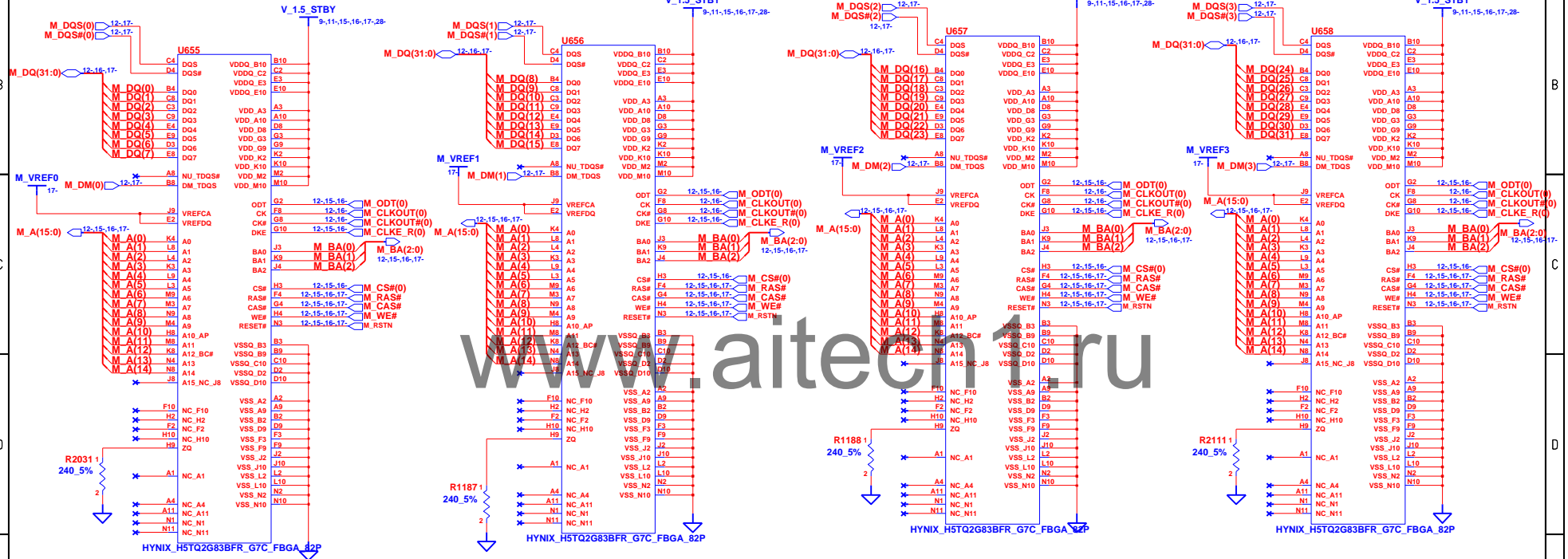
TITLE			
MIMAS			
DDR TERMINATOR			
SIZE	CODE	DOC. NUMBER	REV
A3	CS	6050A2350601	X02

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NOTE: DDR Data pins can be swapped for improved routin according to the following rules:
 1) Data pins can be swapped within each byte
 2) Data bytes can be swapped
 3) DQMx and DQSx must follow each byte

DVT3
CHANGE TO B-DIE



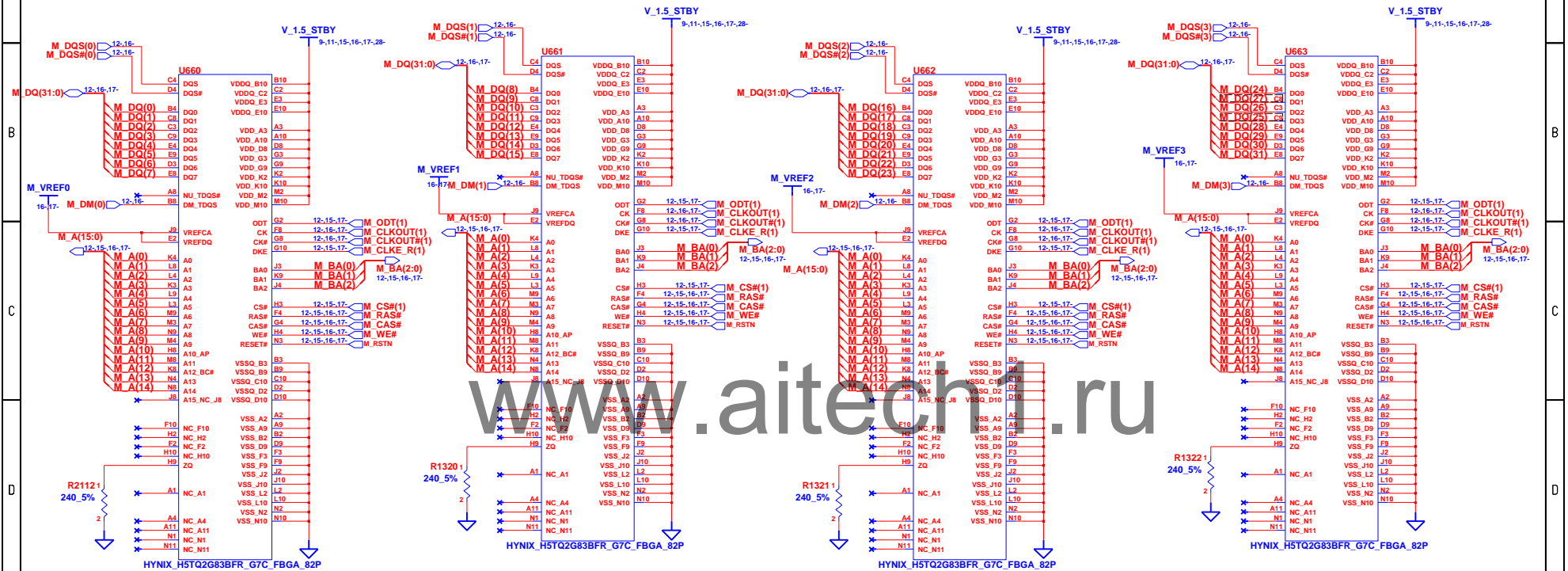
INVENTEC

TITLE			
MIMAS DDR MEMORY			
SIZE	CODE	DOC. NUMBER	REV
A3	CS	6050A2350601	X02
SHEET		16	OF 34

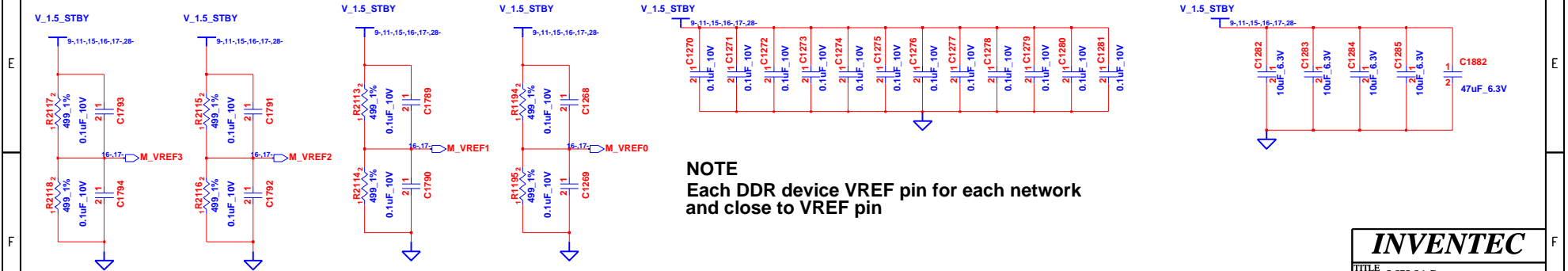
CHANGE by *Drawer Name* 2-Jun-2010

NOTE: DDR Data pins can be swapped for improved routin according to the following rules:
 1) Data pins can be swapped within each byte
 2) Data bytes can be swapped
 3) DQMx and DQSx must follow each byte

DVT3
CHANGE TO B-DIE



NOTE
Each DDR device VREF pin for each network
and close to VREF pin



INVENTEC

TITLE			
MIMAS DDR MEMORY			
SIZE	CODE	DOC. NUMBER	REV
A3	CS	6050A2350601	X02
SHEET		17	OF 34

CHANGE by *Drawer Name* 16-Mar-2010

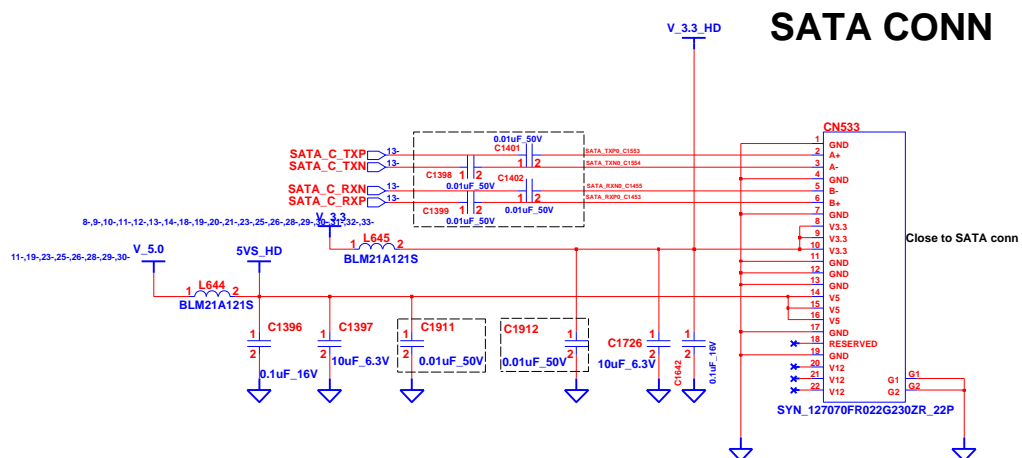
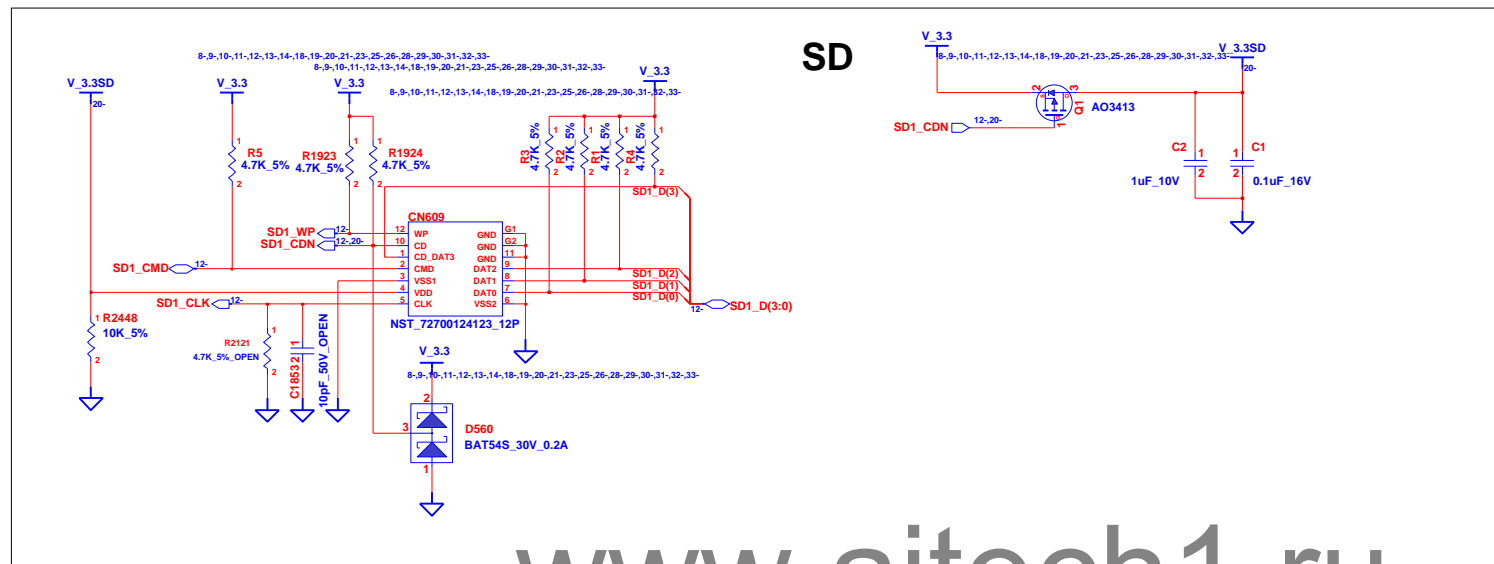
Desktop SKU#2 (DVI ONLY)

The diagram illustrates the PCB layout for a desktop system, specifically for the DVI output. Key components and connections include:

- Connectors:** DVI_TX1, DVI_TX2, DVI_TX0, DVI_TXC, DVI_L_TX1, DVI_L_TX2, DVI_L_TX0, DVI_L_TXC, TW_SCK_DVI, TW_SDA_DVI, TW_SCK_OPT2, TW_SDA_OPT2, VGA_R_DVI, VGA_G_DVI, VGA_B_DVI, VGA_RSNC_DVI.
- Power and Grounding:** V.3.3, V.5.0, +VSS_DVI, FUSE3 (1A 32V), C1259 (1uF 10V), C1851 (10pF 50V), C1852 (10pF 50V), C1810 (1uF 6.3V), C1253 (0.1uF 16V), C1252 (1uF 6.3V), R2143 (4.7K 5% OPEN), R2146 (4.7K 5%), R2147 (4.7K 5%), R2145 (10K 5%), R2142 (0.5%), R2141 (0.5%), R2144 (0.5%), R2146 (0.5%), R2147 (0.5%), R2148 (0.5%), R2149 (0.5%), R2150 (0.5%), R2151 (0.5%), R2152 (0.5%), R2153 (0.5%), R2154 (0.5%), R2155 (0.5%), R2156 (0.5%), R2157 (0.5%), R2158 (0.5%), R2159 (0.5%), R2160 (0.5%), R2161 (0.5%), R2162 (0.5%), R2163 (0.5%), R2164 (0.5%), R2165 (0.5%), R2166 (0.5%), R2167 (0.5%), R2168 (0.5%), R2169 (0.5%), R2170 (0.5%), R2171 (0.5%), R2172 (0.5%), R2173 (0.5%), R2174 (0.5%), R2175 (0.5%), R2176 (0.5%), R2177 (0.5%), R2178 (0.5%), R2179 (0.5%), R2180 (0.5%), R2181 (0.5%), R2182 (0.5%), R2183 (0.5%), R2184 (0.5%), R2185 (0.5%), R2186 (0.5%), R2187 (0.5%), R2188 (0.5%), R2189 (0.5%), R2190 (0.5%), R2191 (0.5%), R2192 (0.5%), R2193 (0.5%), R2194 (0.5%), R2195 (0.5%), R2196 (0.5%), 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[illegible]

INVENTEC			
TITLE MIMAS DVI CONN			
SIZE A3	CODE CS	DOC. NUMBER 6050A2350601	REV X02
SHEET		19	OF 34



SD & SATA

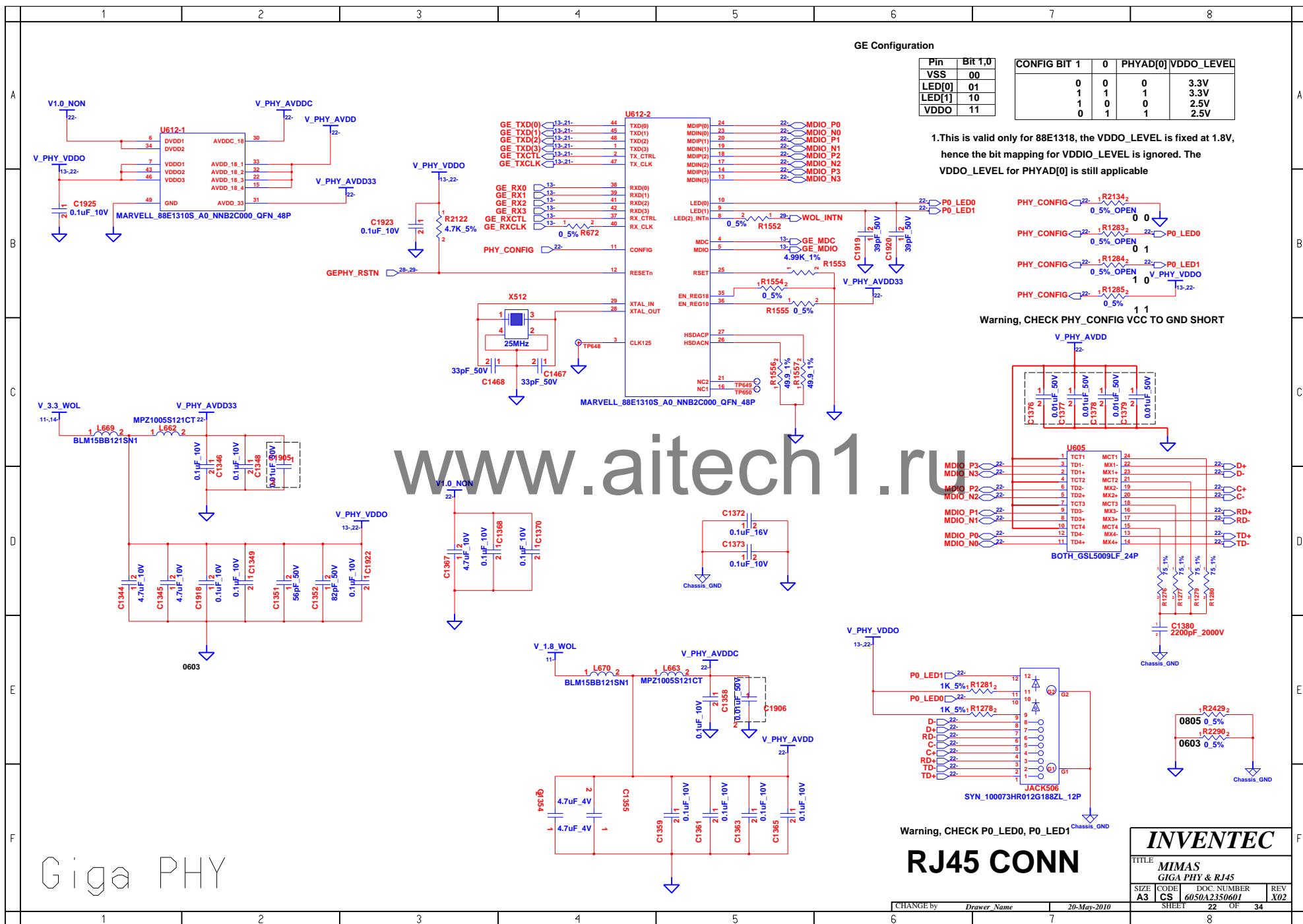
INVENTEC

TITLE	MIMAS SD& SATA CONN
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SIZE	CODE	DOC. NUMBER	REV
A3	CS	6050A2350601	X02
SHEET 20 OF 34			

CHANGE by	<i>Drawer_Name</i>	16-Mar-2010
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3 CS 6050A2350601
SHEET 20 OF 34



305mA

Layout Note : Refer to AN15.17 Rev1.1

Front side

Front side

Back side

Back side

www.aitech1.ru

Int 9 pin

Int 9 pin

WLAN

MINI_CARD

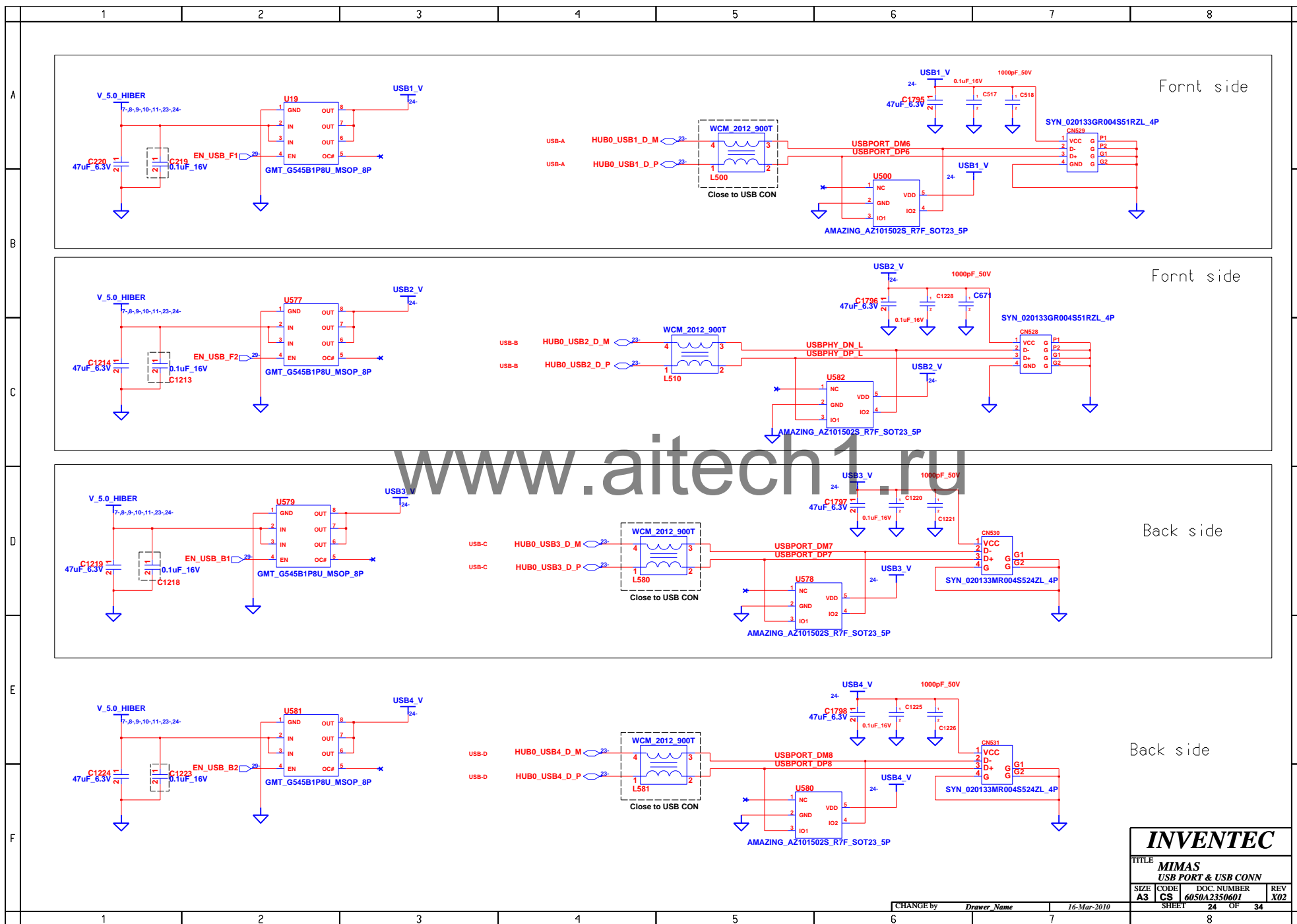
TO 9PIN HEADER

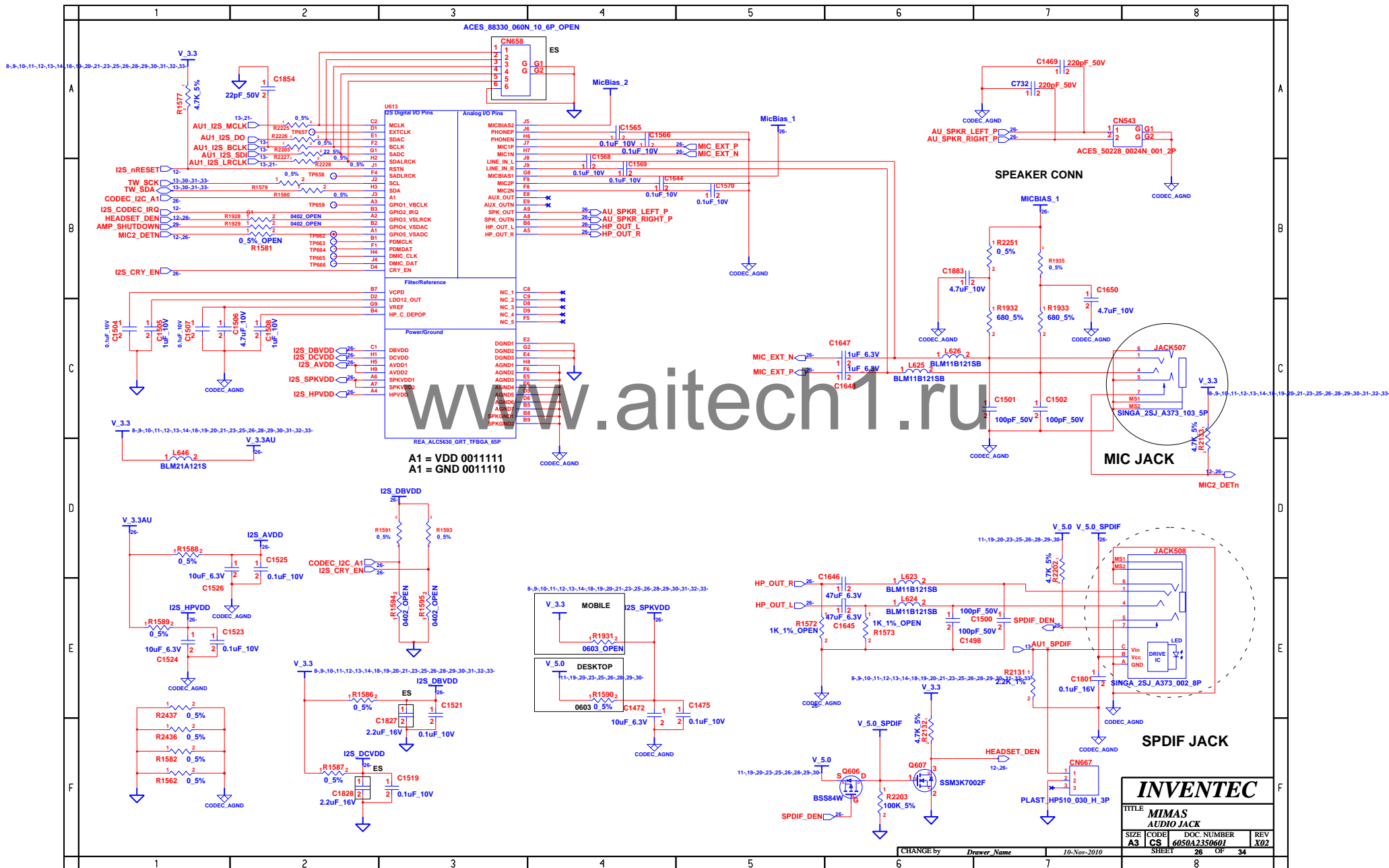
9 PIN USB Header

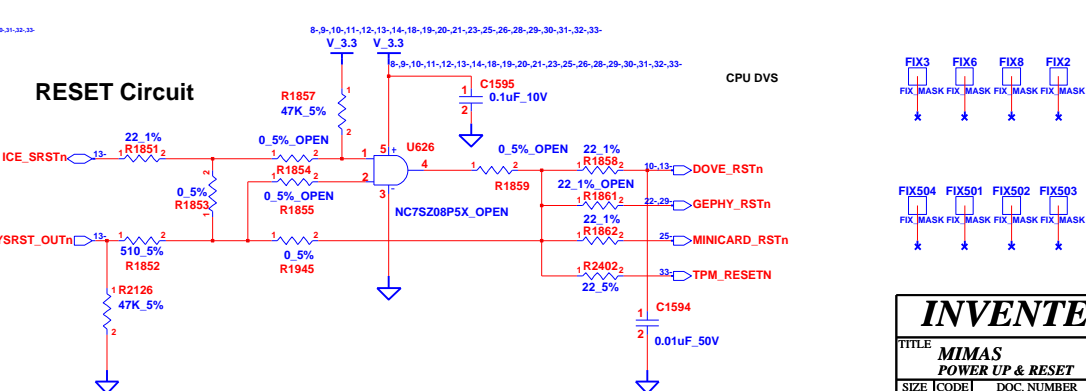
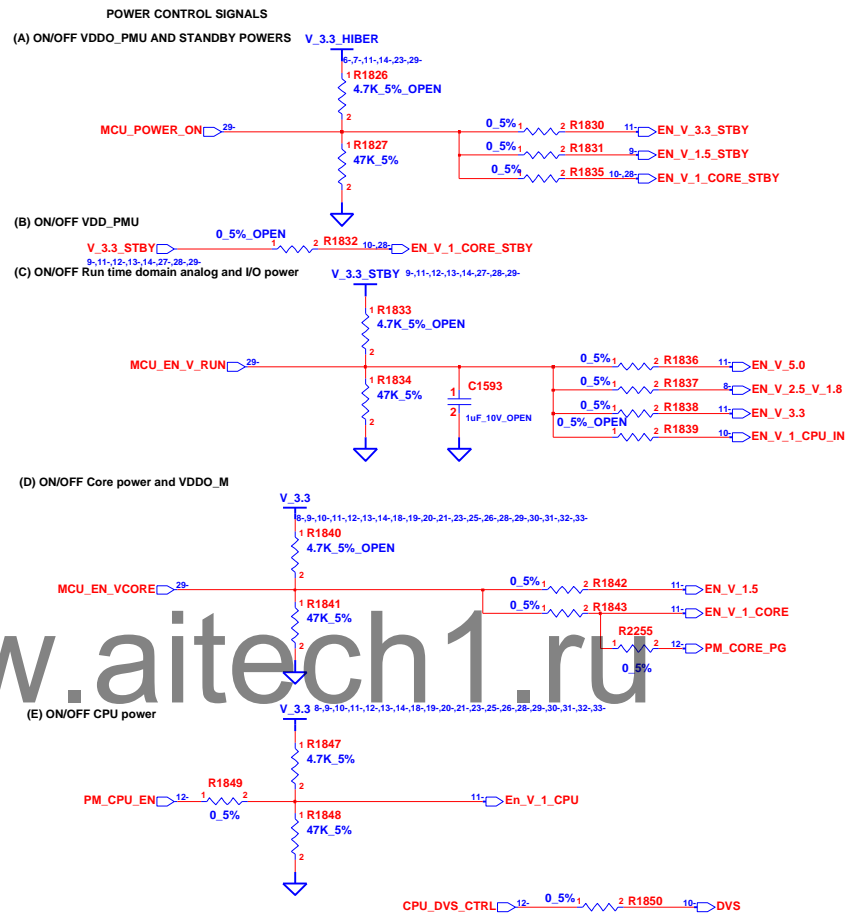
INVENTEC

TITLE
MIMAS
USB HUB & 9-PIN HEADER
SIZE CODE DOC NUMBER REV
A3 CS 6050A2350601 X02
SHEET 23 OF 34

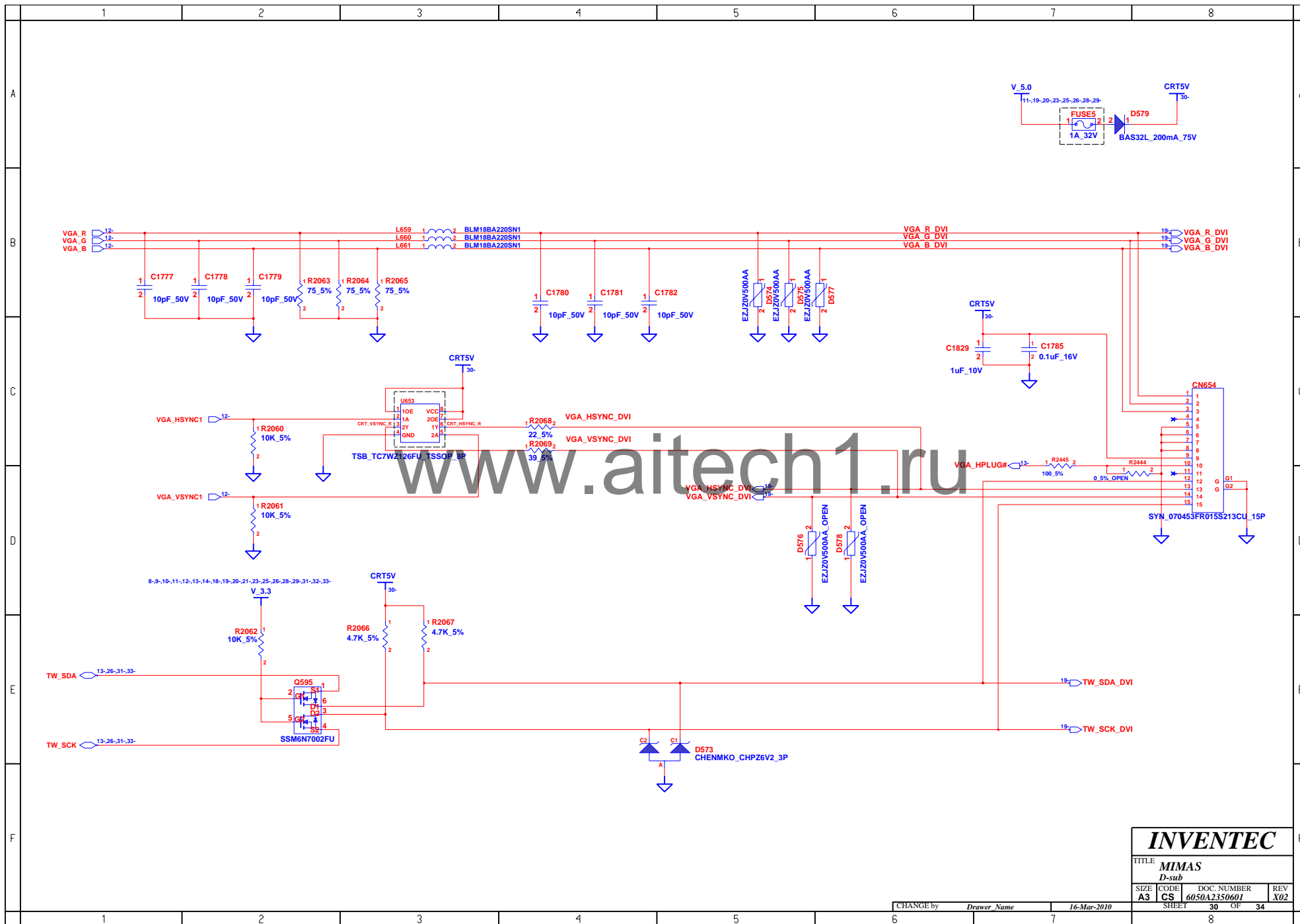
CHANGE by *Drawer Name* 16-Mar-2010







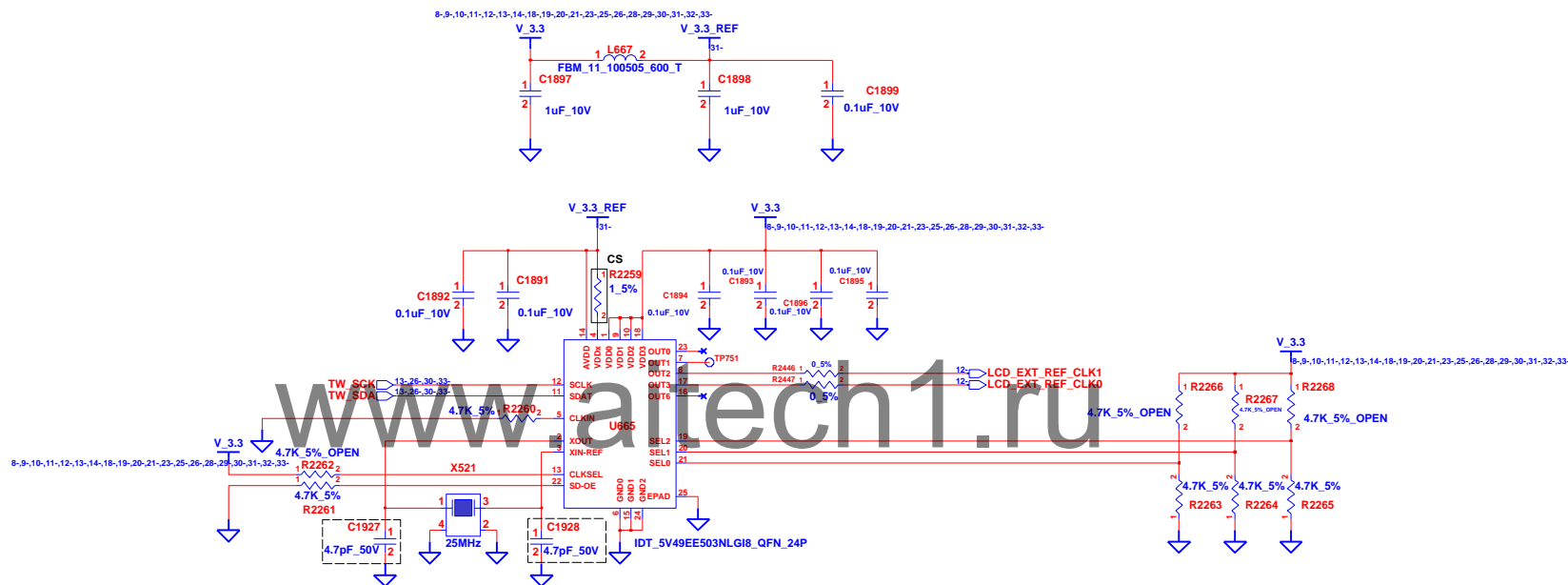
INVENTEC			
TITLE MIMAS POWER UP & RESET			
SIZE A3	CODE CS	DOC. NUMBER 6050A2350601	R M
SHEET 28		OF 34	



INVENTEC

TITLE			
MIMAS			
D-sub			
SIZE	CODE	DOC. NUMBER	REV
A3	CS	6050A2350601	X02
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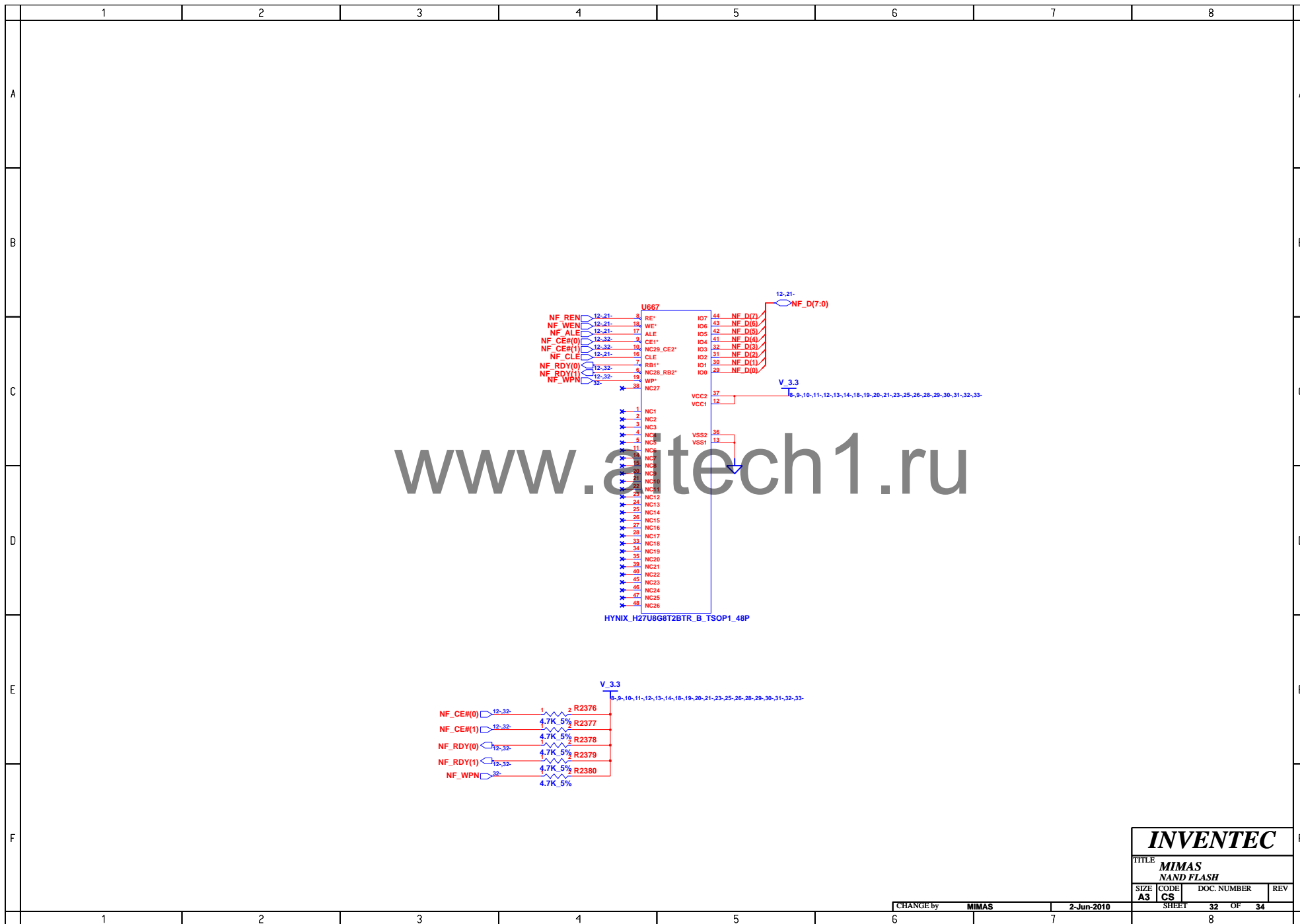


INVENTEC

TITLE MIMAS CLOCK GEN			
SIZE A3	CODE CS	DOC. NUMBER 6050A2350601	REV X02
SHEET 31		OF 34	

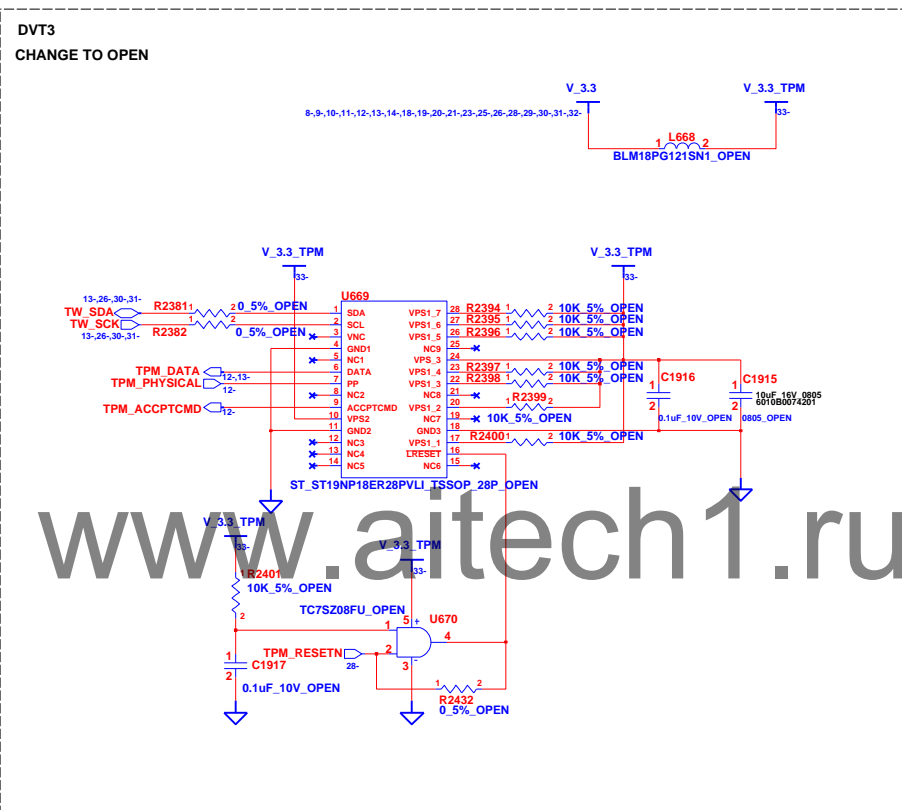
CHANGE by *Drawer Name* 16-Mar-2010

8



INVENTEC			
TITLE			
MIMAS			
NAND FLASH			
SIZE	CODE	DOC. NUMBER	REV
A3	CS	32 OF 34	

CHANGE by MIMAS 2-Jun-2010



INVENTEC			
TITLE			
MIMAS			
TPM			
SIZE	CODE	DOC. NUMBER	REV
A3	CS		
SHEET 33 OF 34			

CHANGE by MIMAS 19-May-2010

